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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
HOGANS, DAVID L

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,817	SEIBEL ET AL.	
	Examin r	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *September 9, 2002,* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Amendment A filed on September 9, 2002.

Status of Claims

Claims 1-23 are presented for prosecution.

Information Disclosure Statement

The Information Disclosure Statement filed on May 31, 2002, has been considered.

Drawings

The proposed drawing corrections filed on September 9, 2002, have been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,159,782 to Xiang et al. in view of 6,274,488 to Talwar et al.

Claims 1, 3 and 9

Xiang et al. teaches: forming an insulation layer over a semiconductor substrate (See column 6 lines 36-67); forming an amorphous silicon layer over top of the insulation layer (See column 7 lines 01-33); introducing a boron or phosphorous dopant

in a top surface of the amorphous silicon layer (See columns 7-8 lines 59-26); and annealing the amorphous silicon layer to initiate crystallization and distribution of the dopants within the gate (See column 8 lines 26-38 and 55-63).

Xiang et al. fails to explicitly teach a radiation beam to heat the amorphous layer.

However, Talwar et al., in column 5 lines 40-58, teaches irradiating a doped amorphous silicon layer with a laser. Further, Talwar et al. teaches that laser irradiation of the doped amorphous region can diffuse dopants and crystallize the amorphous silicon region.

It would have been obvious to one of ordinary skill in the art to modify Xiang's et al. teachings by incorporating laser irradiation of doped amorphous silicon, as taught by Talwar et al., to diffuse dopants within the amorphous silicon region, as well as, crystallize the amorphous silicon region.

Claim 2

Incorporating all arguments of Claim 1 above and noting that Xiang et al. teaches doping the amorphous silicon gate by ion implantation. (See columns 7-8 lines 59-26)

Claims 4, 5, 16 and 17

Incorporating all arguments of Claims 1, 3, 11 and 15 and noting that Xiang et al. fails to explicitly teach a pulsed laser having a wavelength of between 0.1 and 2.0 microns, a temporal pulse width of less than 1 ms, an irradiance between 0.1 and 1000 J/cm2 per pulse, 3 to 10 pulses and a repetition rate of 200 to 400 Hz.

However, Talwar et al., in column 6 lines 12-27, teaches a pulsed laser with a wavelength between 1-2 microns, a temporal pulse width between 1 to 100 nanoseconds, an irradiance between 0.1 and 10 J/cm2, at 3 to 10 pulses and a repetition rate of 200 to 400 Hz. Furthermore, Talwar et al. teaches that the above laser parameters are dependent upon the laser used and the materials affected by the laser. Therefore, the desired results (amorphous silicon crystallization and dopant diffusion) are due to obvious experimentation.

It would have been obvious to one of ordinary skill in the art to modify Xiang's et al. teachings by incorporating the above lasing parameters, as taught by Talwar et al., to achieve the desired results of crystallinity and dopant diffusion. Furthermore, Talwar's et al. functional use of the above laser parameters renders its application obvious.

Claims 6 and 18

Incorporating all arguments of Claims 1 and 11 and noting that Xiang et al. teaches depositing remaining layers such as a gate contact. (See columns 8-9 lines 63-30)

3. Claims 7, 12-14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,159,782 to Xiang et al. in view of 6,274,488 to Talwar et al. further in view of Microchip Fabrication to Van Zant.

Claims 7 and 19

Incorporating all arguments of Claims 1 and 18 and noting that Xiang et al. and Talwar et al. fail to explicitly teach a metal contact comprised of at least one of tungsten, tungsten silicide, tungsten nitride, tantalum, tantalum nitride, titanium, titanium nitride and platinum.

However, Examiner notes that refractory metals (titanium, tungsten and tantalum) and their silicides offer a lowered contact resistance. Examiner further notes that modern circuit design, especially MOS circuits, employ refractory metals or their silicides as conductive layers due to their lower resistivity and lower contact resistance. (See Microchip Fabrication, Peter Van Zant, Fourth Edition, McGraw-Hill Publishing, pages 403-404, 2000)

Therefore, it would have been obvious to one of ordinary skill in the art to modify Xiang et al. and Talwar et al. because modern circuit design employs metal contacts comprised of at least one of tungsten, tungsten silicide, tungsten nitride, tantalum, tantalum nitride, titanium, titanium nitride and platinum.

Claims 12-14

Incorporating all arguments of Claim 11 and noting that Ishida teaches a dopant layer formed by chemical vapor deposition. (See column 4 lines 25-35) Examiner further notes that Ishida fails to explicitly teach a dopant layer formed by sputtering or evaporation.

However, Examiner notes that sputtering and evaporation are known and conventional within the art for vacuum deposited materials. (See Microchip Fabrication, Peter Van Zant, Fourth Edition, McGraw-Hill Publishing, page 411, 2000) Furthermore, sputtering offers the advantage of deposition of the dopant without chemical or compositional change of the dopant and evaporation deposits low energy atoms without damage to the surface substrate.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Ishida because sputtering and evaporation are known and conventional within the art for vacuum deposited materials.

4. Claims 8, 11, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,159,782 to Xiang et al. in view of 6,274,488 to Talwar et al. further in view of 5,966,605 to Ishida.

Claims 8 and 20

Incorporating all arguments of Claims 1 and 11 and noting that Xiang et al. and Talwar et al. fail to explicitly teach an insulation layer comprised by silicon dioxide.

However, Ishida, in column 3 lines 25-27, teaches an insulation layer made from silicon dioxide. Furhter, Examiner notes that silicon dioxide is a good insulating layer because its melting temperature exceeds that of silicon.

It would have been obvious to one of ordinary skill in the art to modify Xiang et al. and Talwar et al. by incorporating a silicon dioxide layer, as taught by Ishida, to provide a thermally stable gate insulating layer.

Claims 11 and 21

Incorporating all arguments of Claim 1 and noting that Xiang et al. and Talwar et al. fail to explicitly teach wherein the dopant layer is formed on top of the amorphous silicon layer.

However, Ishida, in column 4 lines 25-35, teaches a dopant layer formed over a polysilicon gate structure. Further, Ishida teaches that the dopant layer can be laser annealed to promote diffusion of the dopant within the gate electrode.

It would have been obvious to one of ordinary skill in the art to modify Xiang et al. and Talwar et al. by incorporating a dopant layer formed over the amorphous silicon layer, as taught by Ishida, to promote diffusion of the dopant within the gate electrode upon laser annealing.

5. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,159,782 to Xiang et al. in view of 6,274,488 to Talwar et al. further in view of 6,312,998 to Yu.

Claims 10 and 22

Incorporating all arguments of Claims 1 and 11 and noting that Xiang et al. and Talwar et al. fail to explicitly teach a gate height of less than 500 nanometers.

However, Yu, in column 4 lines 39-56, teaches a gate height of 100-200 nanometers. Examiner notes that it is well known and conventional in the art to reduce transistor dimensions to increase device speed. Furthermore, Yu's functional use of a 100-200 nanometer gate renders its application obvious.

It would have been obvious to one of ordinary skill in the art to modify Xiang's et al. and Talwar et al. teachings by incorporating a gate height of 100-200 nanometers, as taught by Yu, to increase device speed.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over 6,159,782 to Xiang et al. in view of 6,274,488 to Talwar et al. further in view of 5,966,605 to Ishida further in view of 6,077,758 to Zhang et al.

Incorporating all arguments of Claim 11 above and noting that Xiang et al and Talwar et al. fail to explicitly teach dopant concentrations of at least one of boron, arsenic and phosphorus up to $3x10^{20}$ ions/cm^3, $5x10^{20}$ ions/cm^3, and $1x10^{21}$ ions/cm^3, respectively.

However, Zhang et al., in column 10 lines 51-55, teaches a doping concentration of phosphorus or boron between 10^{19} and 10^{21} cm^{-3}. Examiner notes that it is known and conventional within the art to dope silicon with boron or phosphorus at concentration levels of 10^{19} to 10^{21} ions/cm^{-3}, to reduce or lower resistivity.

It would have been obvious to one of ordinary skill in the art to modify Xiang's et al. and Talwar's et al. by incorporating the above doping concentrations, as taught by Zhang et al., to lower the resistivity of the device. Furthermore, Zhang's et al. functional use of the above doping concentrations, renders its application obvious.

Response to Arguments

7. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

dh
December 8, 2002

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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